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CSP Reliability for Single- and Double-Sided Assemblies

A JPL-led consortia representing government agencies and private companies pooled in-kind resources to develop the quality and reliability of chip-scale packages (CSPs) for a variety of projects. In the process of building the test vehicles, many challenges were identified.

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A key issue yet to be fully addressed in chip-scale packaging is the matter of interconnection reliability. The main objective of the JPL-led CSP consortium, which included representatives from government agencies and private companies, was understanding quality and assembly reliability issues associated with the implementation of CSPs.

Our experience with implementing CSP technology challenges include design and fabrication of standard and microvia-based boards, as well as the assembly of two types of test vehicles. We will also discuss preliminary thermal cycling test results under four environmental conditions. Finally, we will compare thermal cycling test results for single- and double-sided assemblies to the limited data available in the literature.

CSP Definitions

Although CSP is widely employed by both suppliers and users, its definition has evolved the technology has matured. At the beginning of the package's introduction in the market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers found it difficult to build these packages, and the users had difficulty in accommodating the need for the new microvia printed circuit board, chiefly because of routing requirements and increased PWB cost.

The "expert definition" undermines one of the key purposes of the packages, which is to allow for die shrinkage. If die shrinkage is acceptable for the package to retain its footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

There are many unresolved technical issues associated with CSP implementation. Technical issues also change as packages mature. For example, in early 1997 packages with 1 mm pitch (and lower) were the dominant CSPs. In early 1998, however, packages with 0.8 mm pitch (and lower) became the norm for CSPs. New issues include the use of flip-chip die rather than wire-bond die in the CSP, which may lead to flip-chip failure within the package-a potential new failure mechanism.

JEDEC Survey

Figure 1 shows the results of surveys by JEDEC (Joint Electron Device Engineering Council) and EIAJ (Electronic Industries Association of Japan) team members. Surveys were carried out in 1998 regarding the status of development and production of grid CSPs.1 The JPL-CSP consortium experience on the availability of daisy-chained CSPs for characterization of assembly reliability followed a similar path to JEDEC and EIAJ on package I/O and pitch.

CSP availability and delivery on time was one of the most challenging issues. For example, at the start of the program in early 1997, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O (0.5 mm pitch) package was dropped by the manufacturer prior to the trial test vehicle assembly. Three other packages with higher I/O and 0.5 mm pitch were not delivered.

Two of these were not delivered due to package interposer issues. Another example was a hard metric 0.5 mm CSP package with 188 I/Os, with reliability data provided by the supplier for its English pitch version. The supplier was unable to meet our last build, scheduled in late 1998.

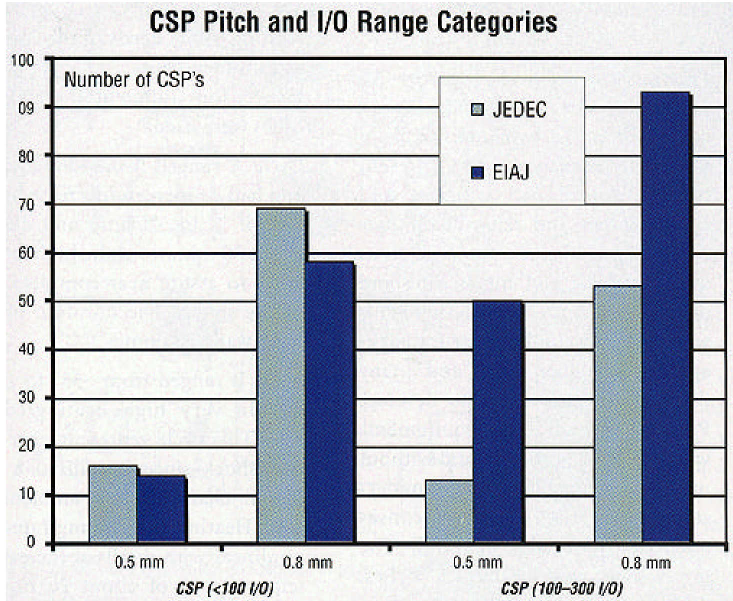


Figure 1. This graph compares EIAJ and JEDEC pitch and I/O ranges in CSPs

The delay and failure to deliver that we experienced clearly indicate that the package suppliers were struggling to build CSPs with 0.5 mm pitch, especially with high I/O counts. The majority of the follow-on program packages, begun in early 1998, feature pitches of 0.8 mm, which are similar to the JEDEC findings. In this later phase, there are a few high I/O CSPs with 0.5 mm pitch. This clearly indicates that industry is starting to be more comfortable moving towards a tighter pitch at higher I/O, which was validated by the survey.

Implementation Challenges

Table 1: CSP Configurations

Package ID	Package Type	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package Thickness (mm)	Ball Diameter (mm)
A	Low I/O Wafer	1.6 x 3.2	0.25 x 0.15	0.5	12	0.5	0.075
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	–
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	96	1.75	0.3
H	CSP-Redistribution-1	10.025 x 8.995	0.254	0.5	96	–	0.3
I	CSP-Redistribution-2	6.22 x 5.46	0.254	0.5	99	–	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
L	TAB CSP-3	13.1 x 13.1	0.3	0.5	188	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	–	0.3

The JPL-led CSP consortia of enterprises representing government agencies and private companies joined to pool in-kind resources for developing the quality and reliability of chip-scale packages (CSPs) for a variety of projects. In the process of building the JPL-led consortia test vehicles,[2] numerous challenges were identified. The thought processes for the first test vehicle began in late 1996, when very few packages were available for evaluation. The design for the second test vehicle was initiated in mid-1998, when a much larger number, nearly 50 types, of CSPs were available.

Although the CSP's rapid growth has eased package availability, its implementation, especially for high reliability applications, requires the establishment of many technical issues including assurance for quality and confidence in reliability, as well as development of the necessary infrastructure. Key test vehicle issues for environmental tests included:

- **Lack of daisy-chained package availability**. CSP availability in daisy chain for attachment reliability characterization was one of the challenging issues at the start of the program in early 1997. Initially, we had planned to test 16 packages with I/Os ranging from 12 to 540. Because of non- delivery, the total number of CSPs tested were reduced to 10 and the densest package featured 275 I/Os.
- **Design guidelines and standards for various CSP elements were not available.** For example, there was no information on pad design relative to package pad for achieving optimum reliability.
- **The need for microvia PWBs**. The standard PWB design could be used for low I/O CSPs. Build-up (microvia) board technology is required for higher I/O CSPs in products with active die. For daisy-chained packages it is possible to design high I/O on a standard board. Board design guidelines are needed, especially for the build-up (micro-via) configuration.
- **I/O Limitations**. There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future (one to three years), the dominant packages would be those with less than 50 I/Os.

CSP Test Vehicle Design

The consortium agreed to concentrate on the following aspects of CSP technology and environmental testing:

- **Package I/O /PWB**. Ten packages with 28 to 275 I/Os, listed in Table 1, were studied. The TSOP was used as the control. PWBs were FR-4 and BT (Bismaleimide Triazine) materials, which were available in the resin, copper coated form and high temperature FR-4. The boards were double-sided, standard and microvia, with four types of surface finishes considered. Organic solder preservative (OSP), hot air solder leveling (HASL), and immersion Au/Ni and silver; the majority were OSP finish.
- **Solder paste/volume**. Three types of solder pastes were included: no-clean, water soluble (WS) and rosin mildly activated (RMA). Three stencil thicknesses were included: high, standard and low. The two extreme thicknesses were four and seven mils with different stencil aperture designs, depending on the pad size. The standard used for the majority of test vehicles was six mil thickness.
- **Package/test vehicle feature-**All packages were daisy chained and contained up two internal chain patterns. Packages had different pitches, solder ball volumes and compositions and daisy-chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os, and many daisy-chain mazes were to develop. Packages with underfill requirements were included both with and without underfill enable a better understanding of the reliability consequences of not using underfill. The test vehicle was 4.5 by 4.5 inches, divided into four independent regions. For single-side assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages.
- **Single- and double-sided assembly.** PWBs were double-sided (microvia and standard) and several boards with double-sided packages were assembled. The use of different microvia and standard PWBs allowed a direct reliability comparison between the standard and microvia technologies, single- and double-sided processing issues, and single- versus double-sided solder joint reliability. In designing daisy chains, it became apparent that standard PWB technology could not be used for routing most packages.

Environmental Testing

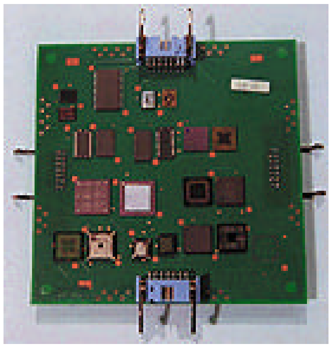


Figure 2. JPL Consortium double-sided test vehicle.

To link the data to those generated for the Ball Grid Array Consortium test, two conditions of -30° to 100° C (cycle A) and 55° to 125° C (Cycle B) were included. Two additional cycles were also investigated. Thermal cycling in the range of 0° to 100° C was performed, according to the needs of the commercial team members.

Hence, four different thermal cycle profiles were used:

- Cycle A ranged from -30° to 100° C and had an increase/decrease heating rate of 2° to 5° C/min and dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.
- Cycle B ranged from -55° to 125° degrees C, with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient and cold. Heating and cooling rates were nonlinear with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.
- Cycle C ranged from -55° to 100° C with a short time duration at low temperature. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes. The duration of each cycle was 90 minutes.
- Cycle D ranged from 0° to 100°C with a 2-5°C/min heating/cooling rate. The Dwell at the extreme temperatures was at least 10 minutes, the cycle duration was 73 minutes.

Monitoring. The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Section 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10 percent of the cycle life.

Full Production

The consortium assembled different test vehicle types. For full production, about 150 test vehicles with the many variables discussed above were built. The photograph of an assembled test vehicle, with its packages face up, is shown in Figure 2. A drawing for the same double-sided test vehicle, in which the back side package outlines are also apparent, is shown in Figure 3. Note that a few packages were mirror-imaged to another package in a double-sided test vehicle.

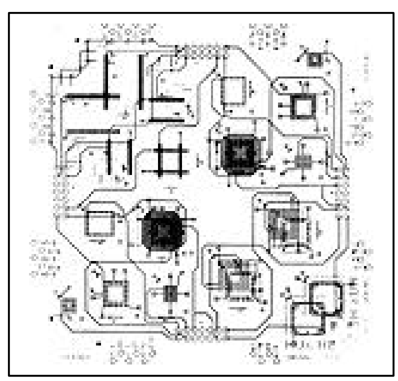


Figure 3. Double-sided test vehicle and regions of package overlap

Environmental Test Results

A large number of assemblies failed, and their cycles to failure were documented. We will examine cycles to failure data for three packages under four thermal cycling conditions. Results for two chip-on-flex assemblies and leadless assemblies on single- and double-sided test vehicles are also presented. Results for other failed and survived assemblies are being gathered and analyzed and will be presented in the future.

Figure 4 compares cycles to failure test results for the "G" package with 99 I/Os under four thermal cycling conditions. The trends are as expected, i.e., as the thermal cycling temperature range increases, the cycles to failure decrease. Note that assemblies failed between 3 to 34 cycles under a near thermal shock in the range of -55° to 125°C (B condition). Cycles to failure was 152 cycles under typical commercial thermal cycling conditions in the ranges of 0 to 10°C. Results for -55/100°C and -30/10°C were between the two extreme cycling conditions.

The data will be used to study the effects of both maximum and minimum temperature changes as well as how well they follow projection models, such as the Coffin-Manson relationship.

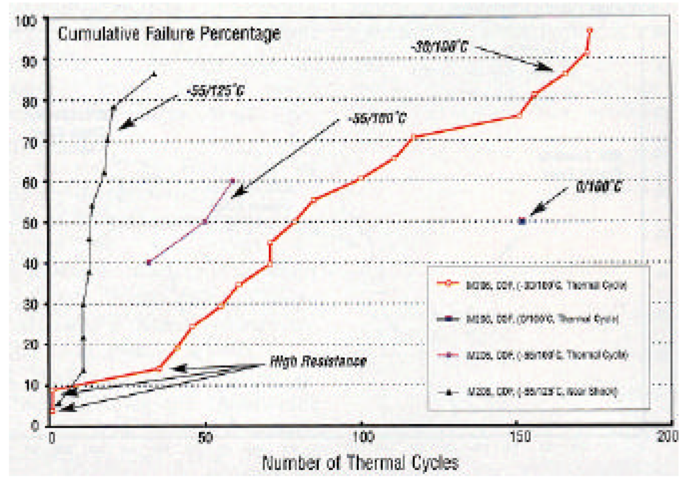


Figure 4. Cumulative failure distribution for flex-on-chip assemblies with 206 I/Os under four thermal cycle conditions.

Figure 5 shows thermal cycling test results for package "B," leadless assembly with 28 I/Os, under two conditions for both single- and double-sided assemblies. The assembly location on the board was such that in a double-sided assembly, it was a direct mirror image of itself with a 90¡ rotation (see Figure 3). The single-sided assemblies failed at much higher cycles than double-sided assemblies. The N50 (cycles to 50 percent failure) were 437 for double and 763 for single sided assemblies under cycle A conditions (-30/100°C). The double-sided assemblies also failed much earlier than single-sided assemblies under other thermal cycling conditions. As an example, results for double-sided assemblies under -55/125°C are also included in the figure.

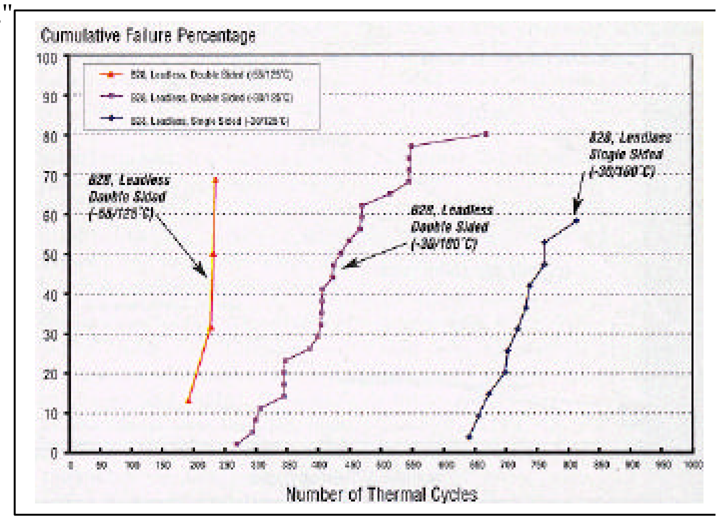


Figure 5. Single- and double-sided assembly failure comparison.

Table 2: Cycles to Failure Percentage Reduction for Double- vs. Single-Sided Assemblies

Double-Sided Conition/Package I/O	Percentage of cycles to failure reduction for double-sided	Reference
1- Mirror imaged/CSP 232 I/O/0.5 mm pitch, PWB thickness=4-layer core, 2-layer build up	50	Sony (3)
2- Mirror imaged/CSP 176 I/O/0.8 mm pitch, PWB thickness=0.8mm	60 (N_{50})	Sharp
3- Same as 2, but with 50% overlap only	40 (N_{50})	
4- Mirror imaged/CSP 144 I/O/0.8 mm pitch, PWB thickness=1.6 mm	50 (N_{50})	Kyocera
5- QFP and CSP mirror imaged, QFP 144 I/O, CSP 308 I/O/0.8 mm pitch, PWB thickness=0.5 mm	20** (increase)	Flextronics
6- Mirror imaged (90° rotation), leadless 28 I/O, PWB thickness=1.3 mm	40 (N50)	JPL (figure 5)

Double-sided assemblies are attractive from the view point of density and electrical improvement. However, they present processing and reliability concerns when assembled. Significant reliability decreases for double-sided assemblies are of great concern, particularly since most CSPs lack the needed reliability when compared to leaded packages. Another minor concern is potential parts fall from the assembled side during second reflow. The CSP's small ball size plus low solder paste volume might not generate enough molten surface tension force to hold the package weight during reflow. This problem can be easily resolved, however, by the use of an adhesive to strengthen the package attachment, even though it may add materials cost, additional process steps and possible contamination

In trying to determine the cause of the early failures of double-sided B28 leadless assemblies, we noticed that this package exactly overlapped another leadless package on the second side with a 90° rotation (see Fig. 3). During visual examination, we noted that the first failure location was at two cross-over corners as shown in Figure 6. These test results, showing early joint failures for double-sided assemblies, are qualitatively in agreement with a few assembly reliability test results reported in the literature and summarized in Table 2.

Up to a 60 percent reduction for CSP double-sided assemblies was reported. Surprisingly, one investigator showed an increase of 20 percent. Kasuga of Sony3 showed a 50 percent decrease in solder joint reliability with mirror image package assemblies. Similar test results were presented for another CSP package by Juso of Sharp.4

The reduction in solder joint reliability seems to be dependent on the package offsets relative to the second side. The maximum reduction of 60 percent was found for mirror package assemblies. When the mirror packages were separated to overlap by 50 percent, the reduction became less severe and decreased to 40 percent. For no overlap the interaction between the top and bottom became zero, representing cycles to failure for a single-sided assembly.

A similar trend was observed for ceramic CSPs (S. Uegaki, S. Sato, Kyocera, private communications) when the overlap condition changed. Several CSP overlap variations, including total overlap or mirror imaged, partial overlap and no overlap were studied.

Double-sided assemblies with mirror package showed the maximum cycles to failure reduction, equivalent to 50 percent. A smaller reduction was found as overlap conditions decreased, comparable to the Sharp data for the plastic CSP. On the other hand, one set of data recently presented at IPC's CSP BGA National Symposium (K. Nakajima, et al.[5] contradicts the above reliability trend for single- and double-sided assemblies. An improvement of 20 percent was realized for CSP on a double-sided assembly. In this case, the CSP was mirror imaged with a QFP package on the second side.

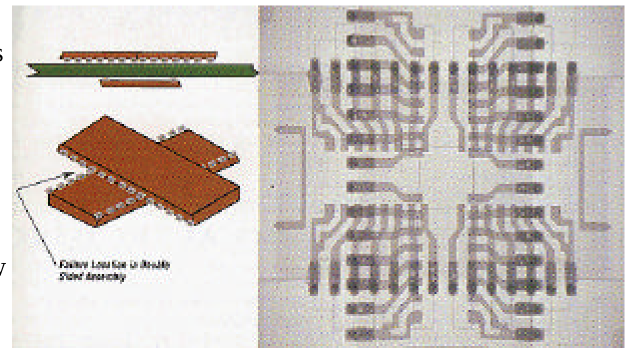
To better define the causes of early failure in double-sided assemblies, their differences to single-sided assemblies need to be examined further. Three main differences are:

- Localized stiffness change due to the second package
- Increase in solder joint height due to package weight during second reßow
- Thermal disturbance-stress induced disturbance from one package to the other, and because of the metallurgy of paste and solder

The combination of solder joint disturbance and an increase in stiffness are the main reasons for a decrease in solder joint reliability for double-sided-assembly. An increase in local stiffness, especially for thinner PWBs, might have a more pronounced effect on its curvature during second reflow, causing a disturbance on the solder joint. A thermal disturbance might also occur due to the metallurgical differences between melting and solidification of solder paste and solder with different compositional phases.

Conclusions

- Cycles to failure for the same assembly under four different environments were different, but the trends were as expected. This means as temperature cycling ranges increased, cycles to failure decreased.
- One package required underfilling, and three others showed very low cycles to failure. Underfilling might be a requirement for these four packages, if it is proven to be effective-even for relatively benign commercial applications.
- The solder joints, disturbed by a second reflow due to back-to-back double-sided assembly, showed early failure. The reduction in cycles to failure was about 40 percent for the leadless package assemblies.



For wider CSP implementation, meaningful reliability data is needed. Accelerated thermal cycling might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analysis are needed to build confidence in assembly reliability.

Thus, understanding the overall philosophy of qualification testing to meet system requirements, as well as detecting new failure mechanisms associated with the CSPs, is the key to collecting meaningful test results and building confidence in the use of this package format.

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